Digital control of a high-coherence fluxonium qubit

WHITEPAPER

Summary

Any truly scalable gate-model quantum computing (GMQC) architecture needs to address the issue of control. Specifically, the number of control lines needed to operate a given quantum processing unit (QPU) must scale slowly with total device count within that QPU. Most proposed superconducting GMQC architectures to date have invoked a brute-force scaling approach to increase QPU size, wherein that line count increases linearly with device count. However, this approach is nearing practical limitations around the scale of 100 physical qubits, which is far below the scale required for building commercially relevant QPUs. In contrast, quantum annealing (QA) QPUs exist today that have been designed with scalability built-in from the outset. This whitepaper describes how D-Wave Quantum Inc. (D-Wave) scalable control technology, as embodied in modern QA QPUs, can be adapted to find utility in the context of superconducting GMQC.

Introduction

Demonstrably functioning superconducting GMQC QPUs containing on the order of 100 physical qubits have been in existence since early 2025 [1, 2]. These QPUs are the latest instantiations of the same brute-force scaling architectures that their developers had used to design smaller QPUs, wherein almost every on-chip device possesses unique bias lines that are controlled by room temperature electronics. However, this approach is expected to become impractical at the scale of thousands of physical qubits. Since useful fault-tolerant GMQC could require on the order of 10 000 000 physical qubits [3], the prospects for brute-forcing all the way to commercial relevance are dim. While laudable efforts have been made using cryogenic CMOS to reduce bias line count from room temperature to an intermediate temperature stage [4], this approach does not resolve the fundamental issue of needing to minimize the bias line count reaching a superconducting QPU held at the lowest temperature stage of a cryogenic system.

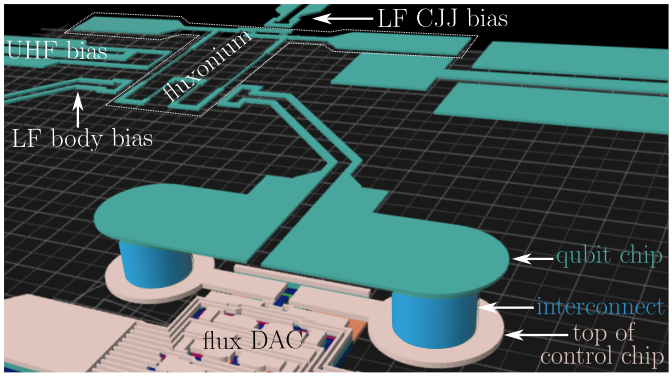

Figure 1: Design of a portion of a flip-chip assembly containing a fluxonium and a flux DAC. Metal on the qubit chip is shown in teal. The top metal layer in the control chip is shown in beige. Superconducting bumps connecting the two chips are shown in blue. An upper shielding layer above the flux DAC on the control chip has been removed and no dielectrics are shown.

In contrast to the state-of-the-art GMQC efforts, the latest generation D-Wave QA QPU contains several thousand flux qubits and tens of thousands of inter-qubit couplers, all of which are controlled with only approximately 300 relatively low-bandwidth bias lines connected to room temperature electronics [5, 6]. Part of the explanation for the large disparity in QPU size between the two approaches to quantum computing is that QA is less demanding to implement than GMQC, thus reducing the complexity of the QPU. A second important factor is that D-Wave made deliberate choices early in QA QPU design to tackle the scalability problem. Significant savings in line counts were achieved by employing approximately 100 000 *on-chip* programmable bias sources that are addressed with about 200 multiplexed control lines. Moreover, these on-chip programmable sources are used to *homogenize* the properties of as-fabricated qubits and inter-qubit couplers such that they can be operated with global control signals as appropriate.

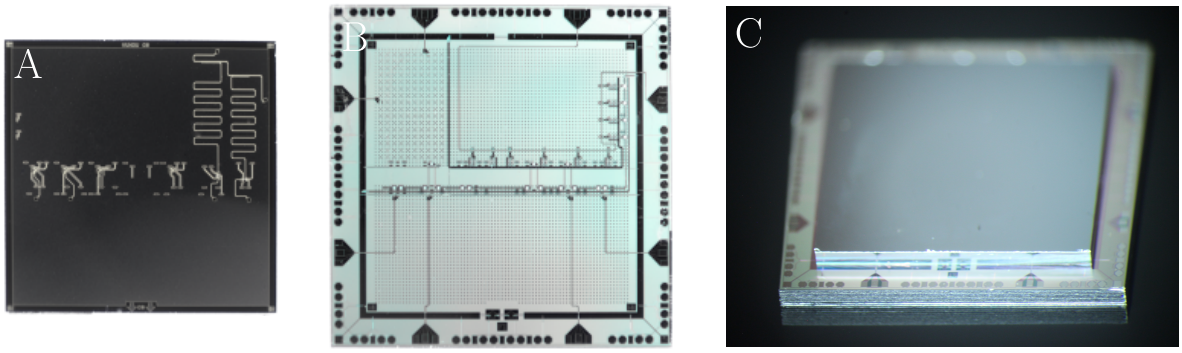

Figure 2: Photographs of a qubit chip (A) and a control chip (B) prior to flip-chip assembly. Superconducting bumps are deposited onto contact pads on both chips, the qubit chip is inverted, and then the matching sets of bumps are compressed together to form the complete flip-chip assembly (C) with a vacuum gap measuring approximately 7 μm between the two chips.

Given D-Wave's success in scaling superconducting QA QPUs and the GMQC community's acute need for scalable control infrastructure, it is reasonable to propose using D-Wave's QA control technology in a future GMQC QPU. For this merging of ideas to be successful, at least two critical issues must be addressed:

1. D-Wave's QA QPUs to date have been implemented in multilayer fabrication stacks containing multiple superconducting metal layers, Josephson junction (JJ) layers, and inter-layer dielectrics. In contrast, most superconducting GMQC hardware efforts use very minimal fabrication stacks consisting of a superconducting bilayer for creating a single JJ layer and a single thick superconducting layer for larger features. How can these approaches be integrated?

2. The key driver for the aforementioned minimal fabrication stack has been the need to maximize qubit coherence. Coupling nominally high-coherence devices to additional control structures could introduce new decoherence mechanisms. Can it be demonstrated that D-Wave's on-chip programmable bias sources need not be coherence-limiting?

D-Wave has addressed both of these questions by manufacturing circuits containing fluxoniums [7, 8], which could be used in future GMQC QPUs [9–12]. The key differentiator between similar circuits made by others is that D-Wave's fluxoniums, that have been fabricated on a chip using a high-coherence minimal fabrication procedure, are partially controlled by programmable bias sources that reside within a separate multilayer chip. These biases are coupled to their target devices using inter-chip superconducting contacts.

3D integrated circuit

The aforementioned minimal fabrication stack, while beneficial for qubit coherence, severely limits options for routing biases, shielding sensitive devices, and increasing circuit density. To partially mitigate these shortcomings, many GMQC efforts have adopted 3D integration [13]. One frequently used technique is flip-chip assembly [14]. Within the context of superconducting GMQC, this involves manufacturing a so-called *qubit chip* using a high-coherence minimal fabrication stack method and a separate so-called *control chip* that may be manufactured using either a single metal layer fabrication stack or a multilayer fabrication stack. The qubit chip hosts the high-coherence devices, namely the qubits and typically the inter-qubit couplers. The control chip hosts the bias lines and contact pads at its periphery that connect to control electronics. Superconducting bumps are then deposited on top of each chip, with the pattern of the bumps being mirror-symmetric. When the qubit chip is flipped upside-down and stacked atop of the control chip, the two bump patterns coincide. The chips are then bonded together under force. Flip-chip bonding was used in the manufacturing of the most notable brute-force scaled superconducting GMQC QPUs to date [1, 2, 15].

D-Wave has manufactured flip-chip assemblies consisting of isolated compound Josephson junction (CJJ) fluxonium [8] on the qubit chip and on-chip programmable bias sources in the control chip. CJJ fluxonium possesses two closed superconducting loops, both of which can be flux biased: the CJJ loop and the body loop. Combinations of flux biases can be used to control the symmetry of the fluxonium potential energy and to adjust the energy spacing of the qubit. The programmable bias sources are digital magnetic flux storage devices referred to as a flux digital-to-analog converters (Φ-DACs) [5]. Φ-DACs are useful as many superconducting devices require static flux offsets to achieve optimal performance. Having many such programmable sources that can be efficiently addressed by a small number of external control lines then reduces the overall line count of large-scale superconducting circuits. Φ-DACs are typically constructed from a plurality of stages, each of which can store many magnetic flux quanta in units of $\Phi_0 \equiv h/2e$, where h is Planck's constant h and e the electron charge. The flux quanta are stored inside inductive loops hosted within the control chip and superconducting shielding ensures there is negligible free space coupling between the storage loops and the fluxonium. In the test circuits described herein, the outputs of the Φ-DACs are galvanically connected to inductive transformers on the qubit chip through superconducting bump bonds. The qubits experience magnetic biases that are proportional to the number of flux quanta stored in each Φ-DACs stage.

An illustration of the metal layers within a portion of a flip-chip assembly is shown in Fig. 1. In this test circuit, the CJJ loop was flux biased using a low-frequency (LF) bias line. The body loop was inductively coupled to 3 separate controls: a shorted ultra-high frequency (UHF) transmission line for driving resonant excitation, a LF bias line for diagnostic purposes, and a Φ-DAC. Photographs of a qubit chip and the top of a control chip are shown in Figs. 2A and 2B, respectively. A photograph of a complete flip-chip assembly is shown in Fig. 2C.

DAC operation

The flip-chip assembly shown in Fig. 2C was cooled in a dilution refrigerator to a temperature $T = 10\,\text{mK}$ for testing. In addition, a witness qubit chip containing an identically designed fluxonium but lacking Φ-DACs and requiring no flip-chip assembly to control was also tested. Similar to previous studies [8], the fluxonium within both circuits exhibited maximum qubit relaxation time $T_1 \sim 200\,\mu\text{s}$ and free induction decay time $T_2^* \sim 20\,\mu\text{s}$ with the qubit the spectral gap tuned to $\Delta/h \sim 200\,\text{MHz}$ via its CJJ flux bias and with its body flux biased to its sweet spot [7]. These observations support the conclusion that an Φ-DAC does not introduce a resolvable increase in decoherence.

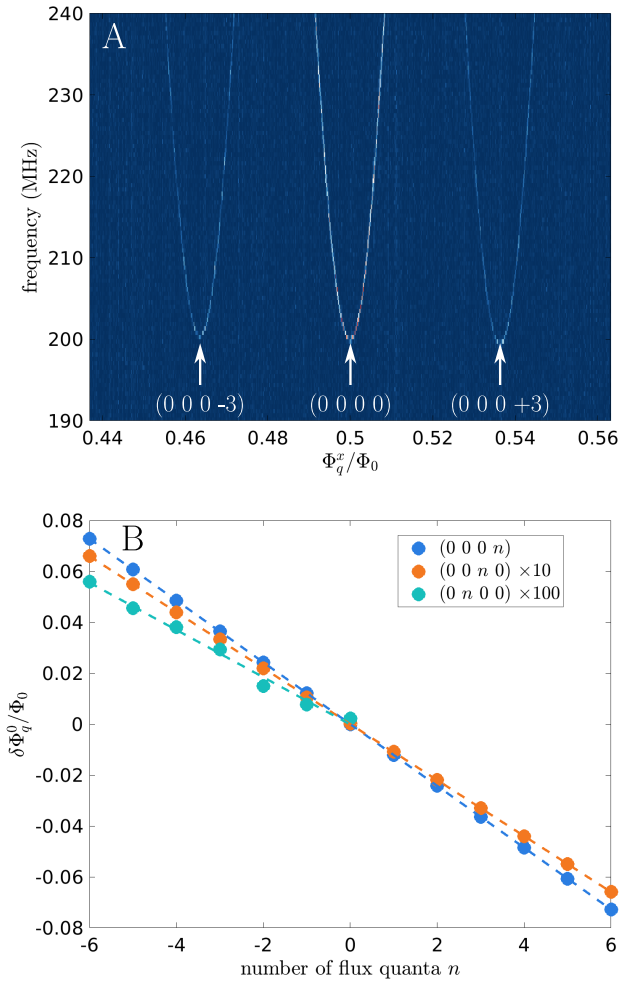

Figure 3: Demonstration of flux DAC operation. (A) Example frequency versus fluxonium body bias Φ_q^x dispersion data for 3 DAC states denoted as $(i\,j\,k\,l)$. (B) Displacements of the minimum in the fluxonium dispersion Φ_q^0 versus number of flux quanta programmed into a given Φ-DAC stage. Data for second and third stage have been multiplied by 100 and 10, respectively.

Operation of a Φ-DAC was confirmed via spectroscopy as a function of DAC state. Example fluxonium dispersion versus LF body bias Φ_q^x are shown in Fig. 3A. The 3 distinct

spectroscopic features correspond to the $0 \rightarrow 1$ excitation of the qubit in the presence of different Φ-DAC *codes*, where the code notation $(i\ j\ k\ l)$ indicates the integer number of flux quanta that have been programmed into each of the 4 stages of the Φ-DAC. Note that both positive- and negative-polarity flux quanta are allowed. The magnitude of the flux bias applied via the Φ-DAC to the fluxonium body is stepped down from integer flux quanta to a much smaller quantity via a ladder of inductances between the storage inductor and the output transformer. The data shown in Fig. 3A illustrate how the fluxonium's sweet spot, corresponding to the minimum of the dispersion and denoted as Φ_q^0 herein, can be translated as a function of Φ_q^x using the Φ-DAC. Mapping the motion of Φ_q^0 as a function of DAC code provides a means to calibrate the flux DAC step size for each stage. Figure 3B shows a summary of these results for 3 of the 4 Φ-DAC stages. Fitting each set of data to a straight line indicates these stages can translate Φ_q^0 by $(12.134 \pm 0.004)\,\mathrm{m}\Phi_0$, $(1.099 \pm 0.004)\,\mathrm{m}\Phi_0$, and $(95 \pm 10)\,\mu\Phi_0$ per stored flux quantum. Further, each stage can hold at least ± 6 flux quanta, which is enough to ensure that the full range output of a given stage spans one translation step of the next-largest output stage. The Φ-DAC then covers a flux bias range set by the largest stage with an accuracy set by the smallest stage.

Perspective

The flip-chip assembly described herein facilitated the union of fluxonium qubits with D-Wave flux-based control circuitry. Moreover, that control circuitry was observed to have no resolvable impact on qubit coherence.

While the demonstrated operation of a flux DAC coupled to a fluxonium involves relatively simple physics, the consequences for practical implementation of superconducting GMQC at scale could be profound. Flux-biased superconducting devices invariably experience flux offsets arising from nearby trapped flux, magnetic defects, or superconducting phase differences due to JJ asymmetries . Such offsets need to be compensated and some superconducting devices require specific nonzero values of applied flux to achieve optimal performance. D-Wave's multiplexed on-chip digital flux control provides an efficient means to apply a very large number of such compensating biases. Consequently, it could be an important factor in enabling future generations of superconducting GMQC hardware.

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